



DOMAIN TECHNOLOGIES INC.

Users Guide Version 1.1

SB-USB2

Emulator

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1 Introduction

The SB-USB2 emulator enables efficient and productive embedded software debugging for the DSP560xx, DSP561xx, DSP563xx, and the DSP568xx. Both compact and portable, it utilizes the JTAG and/or OnCE (On-Chip Emulation) protocols. This versatile probe supports several connector configurations: 2 JTAG connections; 2 OnCE connections; or an individual JTAG and OnCE connection. In addition, the SB-USB2 supplies benchmark timers.

When used with Domain Technologies' BoxView or BoxView IDE debugger, the SB-USB2 provides access to the JTAG device's boundary scan functionality (BSDL file required). Boundary scan operations enable non-intrusive monitoring of the target device pins, even while the target device is executing its own application code. The SB-USB2 emulator can program external flash memory devices also.

With the use of Domain Technologies BoxServer connectivity software, the SB-USB2 emulator can be used for multi-core and/or multi-device development when the JTAG devices are properly connected within the same JTAG scan chain. This development capability allows simultaneous start/stop/single-step for multiple devices; BoxServer connectivity software provides access via TCP/IP connection.

1.1 Package Contents

The SB-USB2 ships with the following:

- Emulator
- USB cable
- Drivers for MS Windows
- Users Guide

1.2 Features

The SB-USB2 has the following features:

- Powered by USB port
- Benchmark Timers
- Freescale On-Chip Emulation OnCE support
- JTAG TAP Debug support
- JTAG Boundary Scan (IEEE1149.1) support
- Logic Levels: 3.3V, 2.5V, 1.8V
- TCK: 32kHz - 10MHz
- Device Power Detection
- Supplies max of 300mA

1.3 Related Components

Domain Technologies features several evaluation boards to promote fast and reliable prototyping. External connectors provide the option for increased performance utilizing the SB-USB2, USB-EMU, and SB-USB emulators. For more information contact Domain Technologies or review www.domaintec.com.

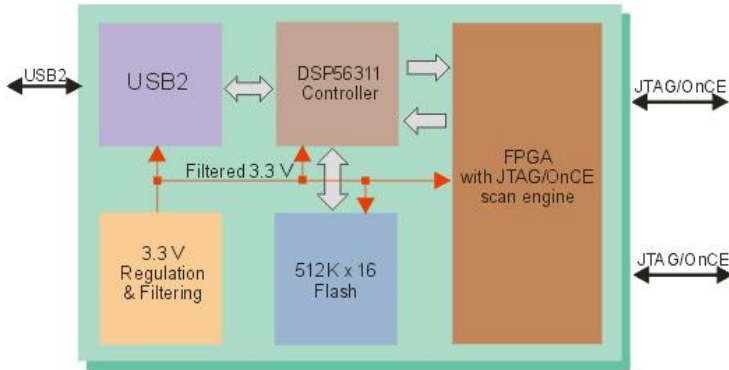
2 Installation

Included with the SB-USB2 emulator is a 6-ft. USB cable, 24 pin to 14 pin ribbon cable and an installation CD. Verify all have been delivered with the emulator. The installation CD contains a number of emulator test program and driver DLLs; these enable the SB-USB2 emulator to operate with Domain Technologies' BoxView and BoxView Integrated Development Environment (IDE) as well as Altium's Crossview Debugger. The software installation must be executed before connecting USB emulator to the system. The installation procedure provides information about location of the USB drivers, so Windows can find them automatically.

Insert the installation CD into your CD ROM drive. If auto detect is enabled in your system environment setup, then the installation program will automatically launch. Otherwise, double-click the *SBUSB2Install.exe* file located on the CD drive from within Windows Explorer. Follow the steps through the installation program to perform a complete or partial install of the SB-USB2 supporting software.

3 Operation of the SB-USB2

The SB-USB2 probe is powered by the USB connection, making it ideal for use by notebook computers or lab environments. In addition, it can detect whether or not the device has power, and can also supply up to 200mA of power to the target device.



The emulator provides benchmark timers: for the OnCE connection, the negative pulse coming over DSO stops the timer; for the JTAG connection, the -DE signal stops the timer. The JTAG interface can be configured to operate with logic levels of 3.3V, 2.5V, or 1.8V. The JTAG clock can be configured between 32kHz and 10MHz. A flexible ribbon cable provides the JTAG or OnCE interfaces with several supported configurations: 2 JTAG (primary and secondary connector); 2 OnCE (primary and secondary connector); or a single JTAG and OnCE connection.

3.1 OnCE Pin-outs

The following pin-out configurations are used with an OnCE connection.

Primary:

DSI	1	2	MUX1
DSO	3	4	GND
DSCK	5	6	GND
-DR	7		key
-RST	9	10	nc
VCC	11	12	nc
nc	13	14	MUX2

Secondary:

DSI	1	2	MUX1
DSO	3	4	GND
DSCK	5	6	GND
-DR	7		key
-RST	9	10	nc
nc	11	12	nc
nc	13	14	nc

3.2 JTAG Pin-Outs

The following pin-out configurations are used with a JTAG connection.

Primary:

TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
nc	7		key
-RST	9	10	TMS0
VCC	11	12	TMS1
-DE	13	14	-TRST

Secondary:

TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
nc	7		key
-RST	9	10	TMS0
nc	11	12	nc
nc	13	14	nc

4 Jumper and Switch Information

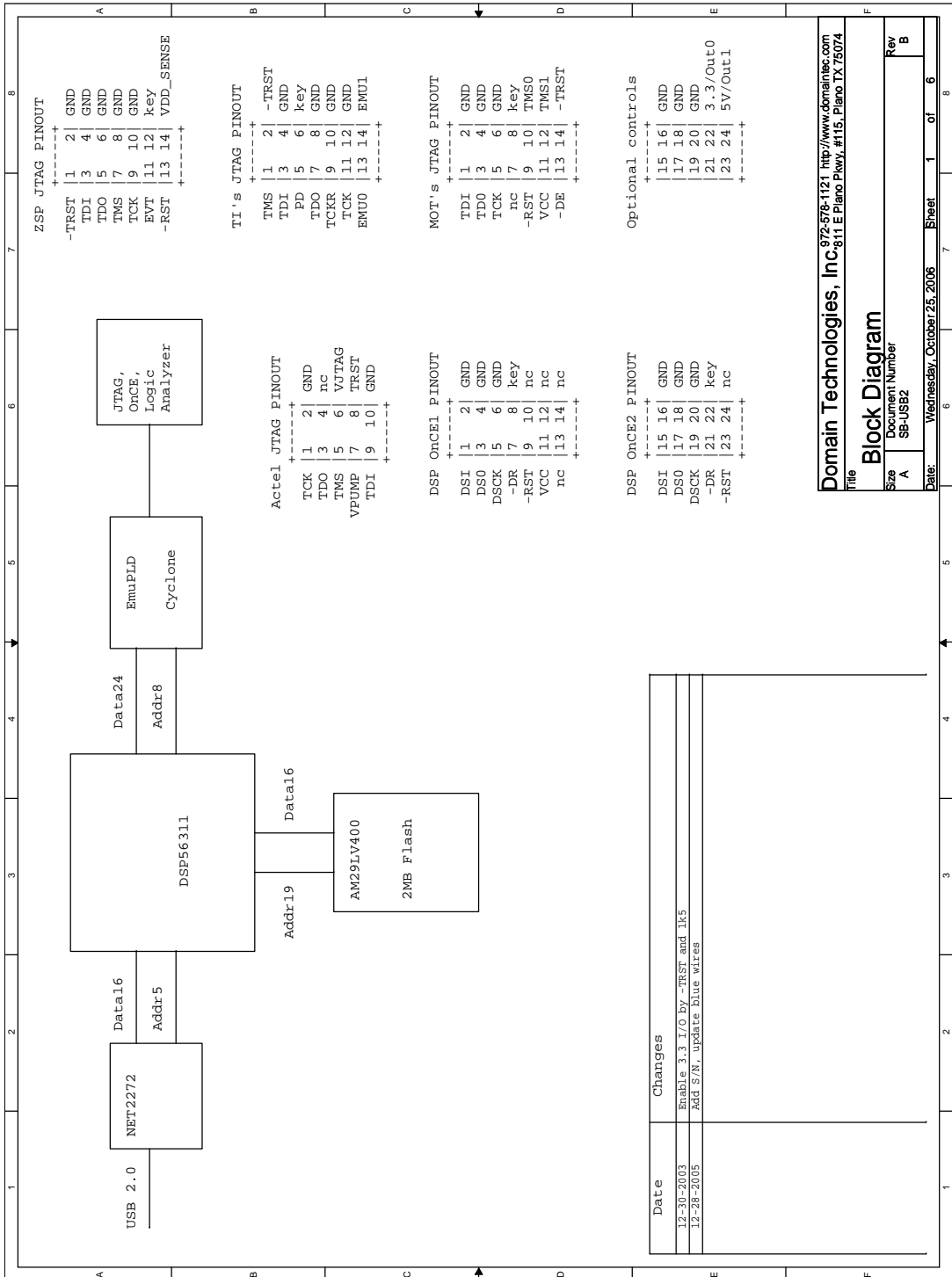
The following table describes the assignment of switches for the SB-USB2's 24 pin IDC connector. Switch 1 is on the top (close to LEDs):

Switch	Connector Position	Left	Right
Sw1	2	I/O	Gnd
Sw2	4	I/O	Gnd
Sw3	6	I/O	Gnd
Sw4	8	I/O	Gnd
Sw5	11	I/O	VCIO
Sw6	16	I/O	Gnd
Sw7	18	I/O	Gnd
Sw8	20	I/O	Gnd
Sw9	22	I/O	VCIO
Sw10	24	I/O	+5V

Note the following jumper information:

Jumper	Location	Description
J13	Bottom Side	Enable power from external power jack
J15	Under USB Connector	1-2 Enable power from USB

For the logic analyzer operation, at least one of the switches needs to provide the ground connection - unless the signal ground is provided externally; for example, to pin #4 of the J15.



ZSP JTAG PINOUT

-TRST	1	2	GND
TDI	3	4	GND
TDO	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
EVT	11	12	key
-RST	13	14	VDD_SENSE

TI's JTAG PINOUT

TMS	1	2	-TRST
TDI	3	4	GND
PD	5	6	key
TDO	7	8	GND
TCKR	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1

MOT's JTAG PINOUT

TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
nc	7	8	key
-RST	9	10	TMS0
VCC	11	12	TMS1
-DE	13	14	-TRST

Optional controls

15	16	GND
17	18	GND
19	20	GND
21	22	3.3/Out0
23	24	5V/Out1

Actel JTAG PINOUT

TCK	1	2	GND
TDO	3	4	nc
TMS	5	6	VJTAG
VPUMP	7	8	TRST
TDI	9	10	GND

DSP OnCE1 PINOUT

DSI	1	2	GND
DS0	3	4	GND
DSCK	5	6	GND
-DR	7	8	key
-RST	9	10	nc
VCC	11	12	nc
nc	13	14	nc

DSP OnCE2 PINOUT

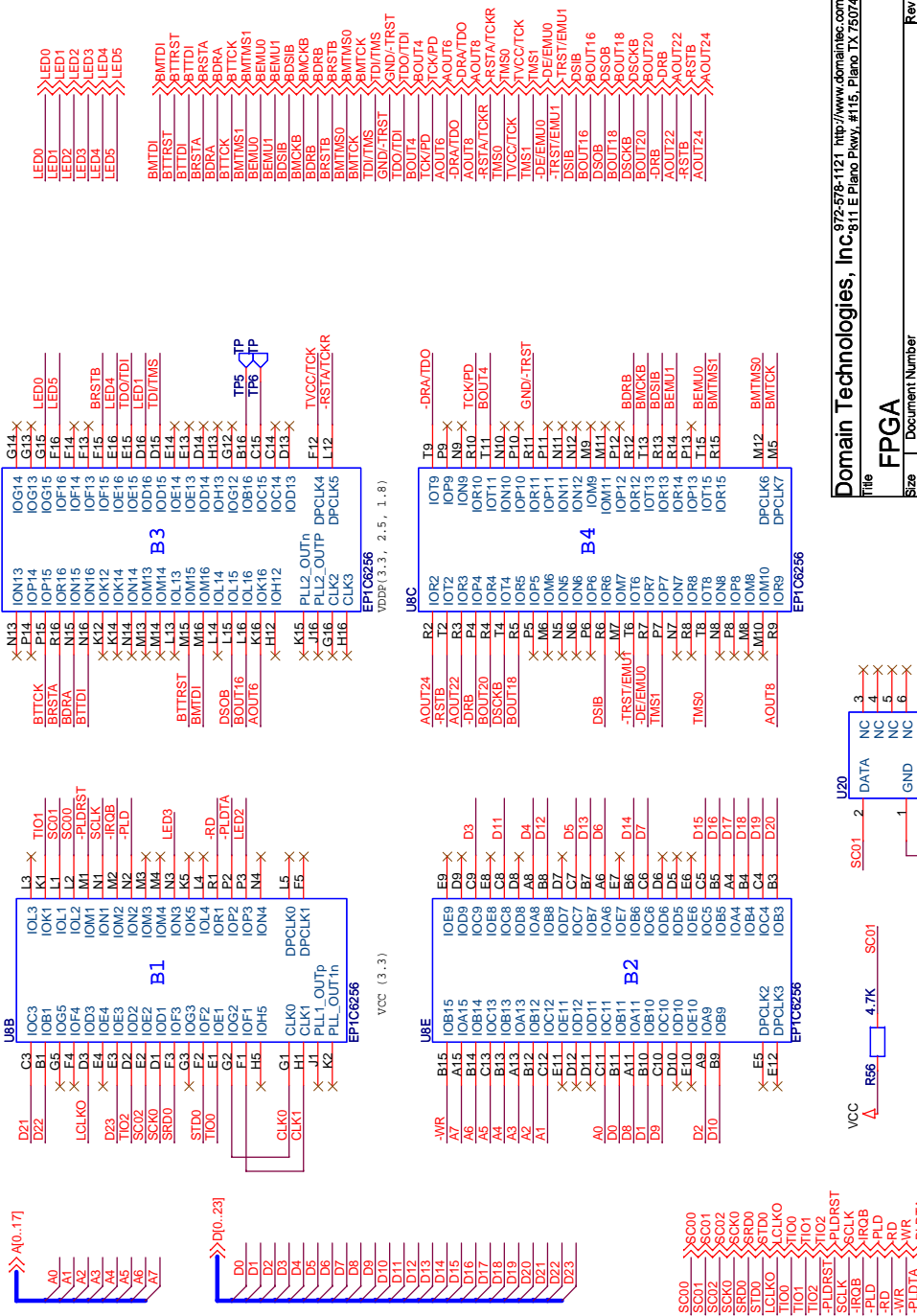
DSI	15	16	GND
DS0	17	18	GND
DSCK	19	20	GND
-DR	21	22	key
-RST	23	24	nc

Date	Changes
12-30-2003	Enable 3.3 I/O by -TRST and Ik5
12-28-2005	Add S/N, update blue wires

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 811 E Plano Pkwy, #115, Plano TX 75074

Title
 Block Diagram

Size	Document Number
A	SB-USBZ
Date:	Wednesday, October 25, 2006
Sheet	1 of 6
Rev	B



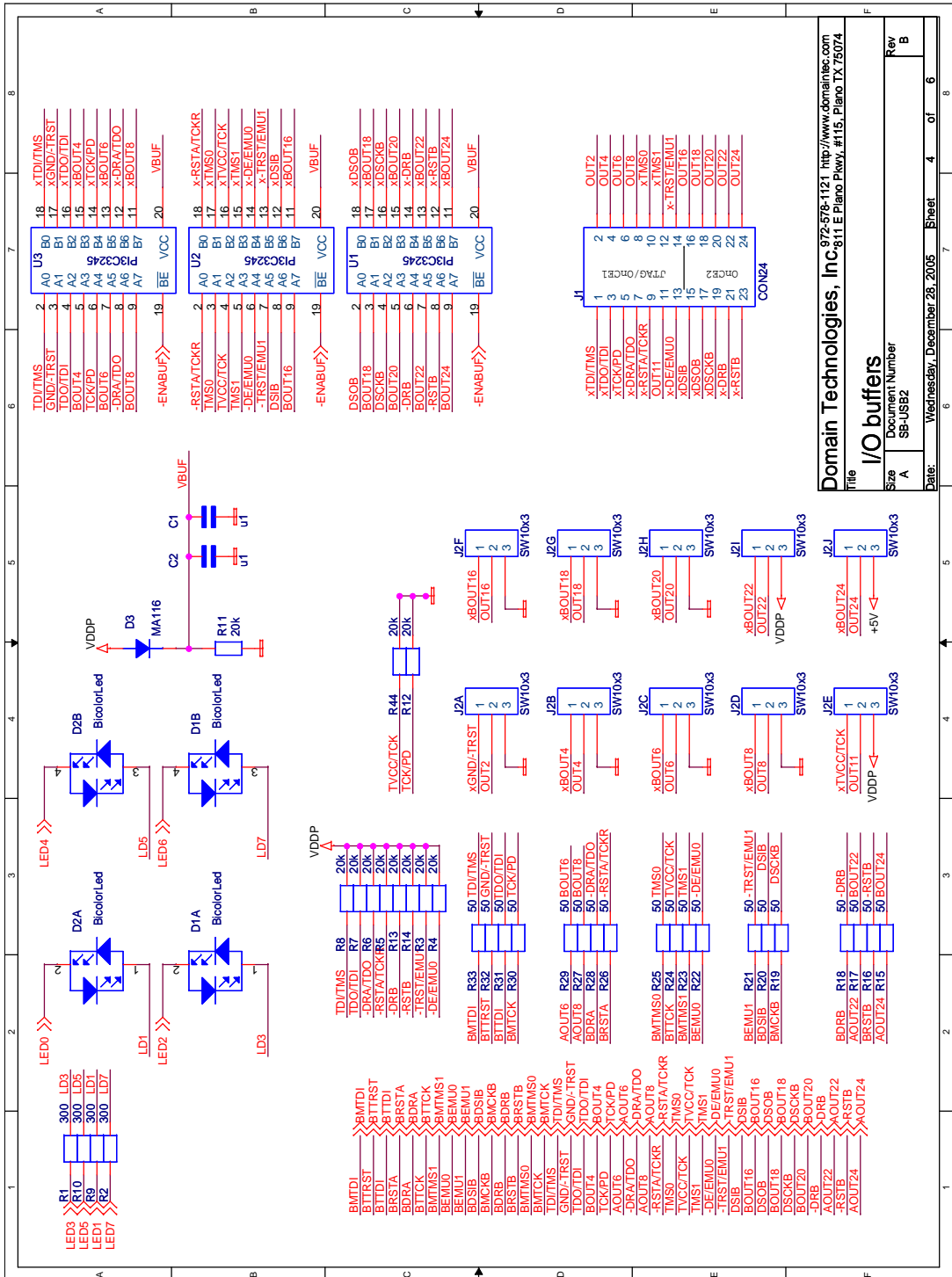
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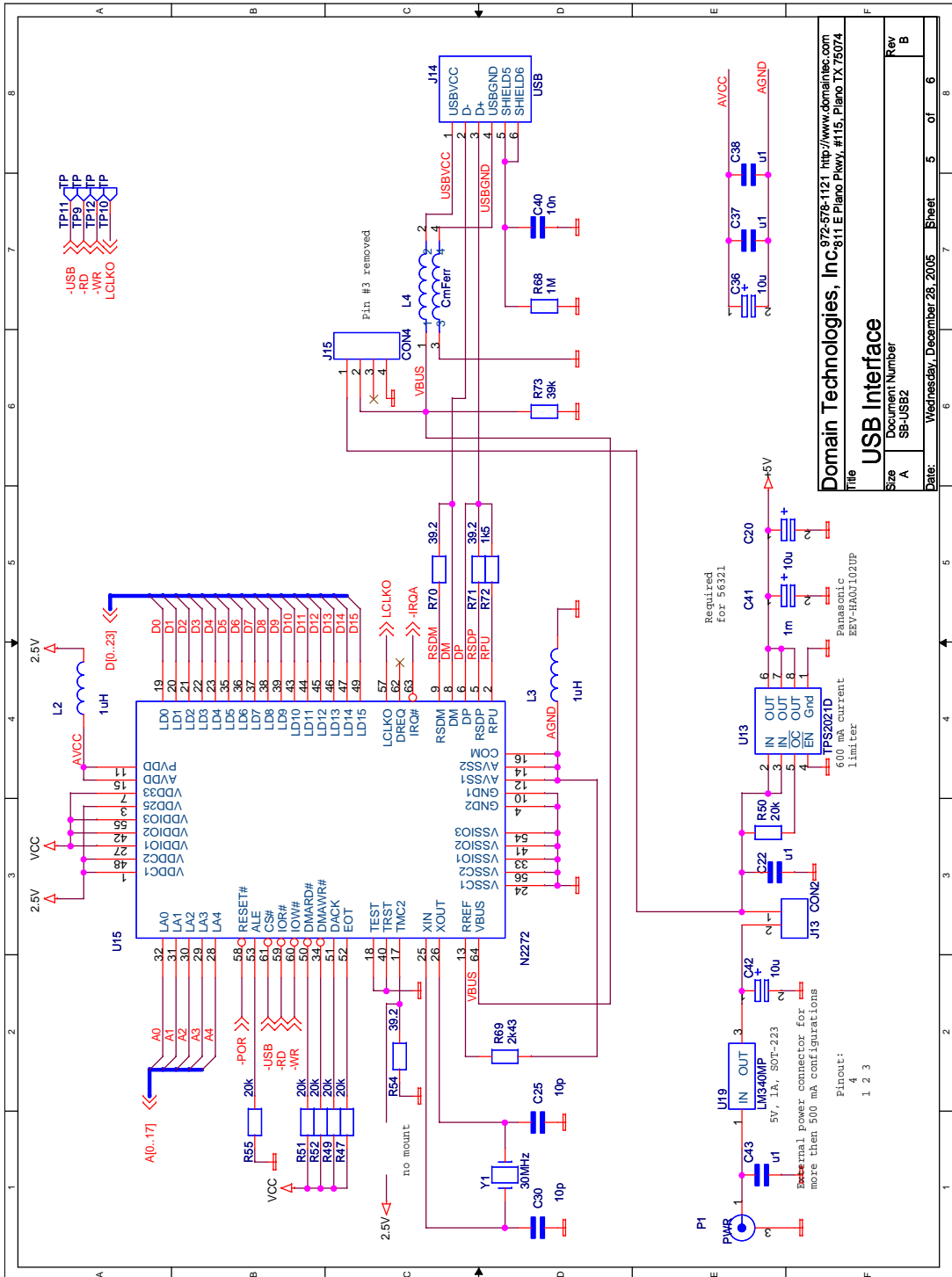
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|------------|----|
| >>>A0..171 | A0 |
| >>>A1..171 | A1 |
| >>>A2..171 | A2 |
| >>>A3..171 | A3 |
| >>>A4..171 | A4 |
| >>>A5..171 | A5 |
| >>>A6..171 | A6 |
| >>>A7..171 | A7 |
- | | |
|-------------|-----|
| >>>D0..231 | D0 |
| >>>D1..231 | D1 |
| >>>D2..231 | D2 |
| >>>D3..231 | D3 |
| >>>D4..231 | D4 |
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| >>>D22..231 | D22 |
| >>>D23..231 | D23 |

- B1**
- | | |
|------|-----------|
| C3 | IOC3 |
| B1 | IOB1 |
| X G5 | IOG5 |
| X G6 | IOG6 |
| X F4 | IOF4 |
| D3 | IOD3 |
| X E4 | IOE4 |
| X E5 | IOE5 |
| X F1 | IOF1 |
| X F2 | IOF2 |
| X G1 | IOG1 |
| X G2 | IOG2 |
| X G3 | IOG3 |
| X G4 | IOG4 |
| X H1 | IOH1 |
| X H2 | IOH2 |
| X H3 | IOH3 |
| X H4 | IOH4 |
| X H5 | IOH5 |
| G1 | CLK0 |
| H1 | CLK1 |
| J1 | PLL1_OUTp |
| X K2 | PLL_OUTin |
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| A7 | IOA15 |
| A6 | IOA14 |
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| X D160 | IOD160 |
| X D161 | IOD161 |
| X D162 | IOD162 |
| X D163 | IOD163 |
| X D164 | IOD164 |
| X D165 | IOD165 |
| X D166 | IOD166 |
| X D167 | IOD167 |
| X D168 | IOD168 |
| X D169 | IOD169 |
| X D170 | IOD170 |
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| X D200 | IOD200 |
| X D201 | IOD201 |
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| X D204 | IOD204 |
| X D205 | IOD205 |
| X D206 | IOD206 |
| X D207 | IOD207 |
| X D2 | |



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 Title: I/O buffers
 Size: Document Number
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 Date: Wednesday, December 28, 2005 Sheet 4 of 6
 Rev B

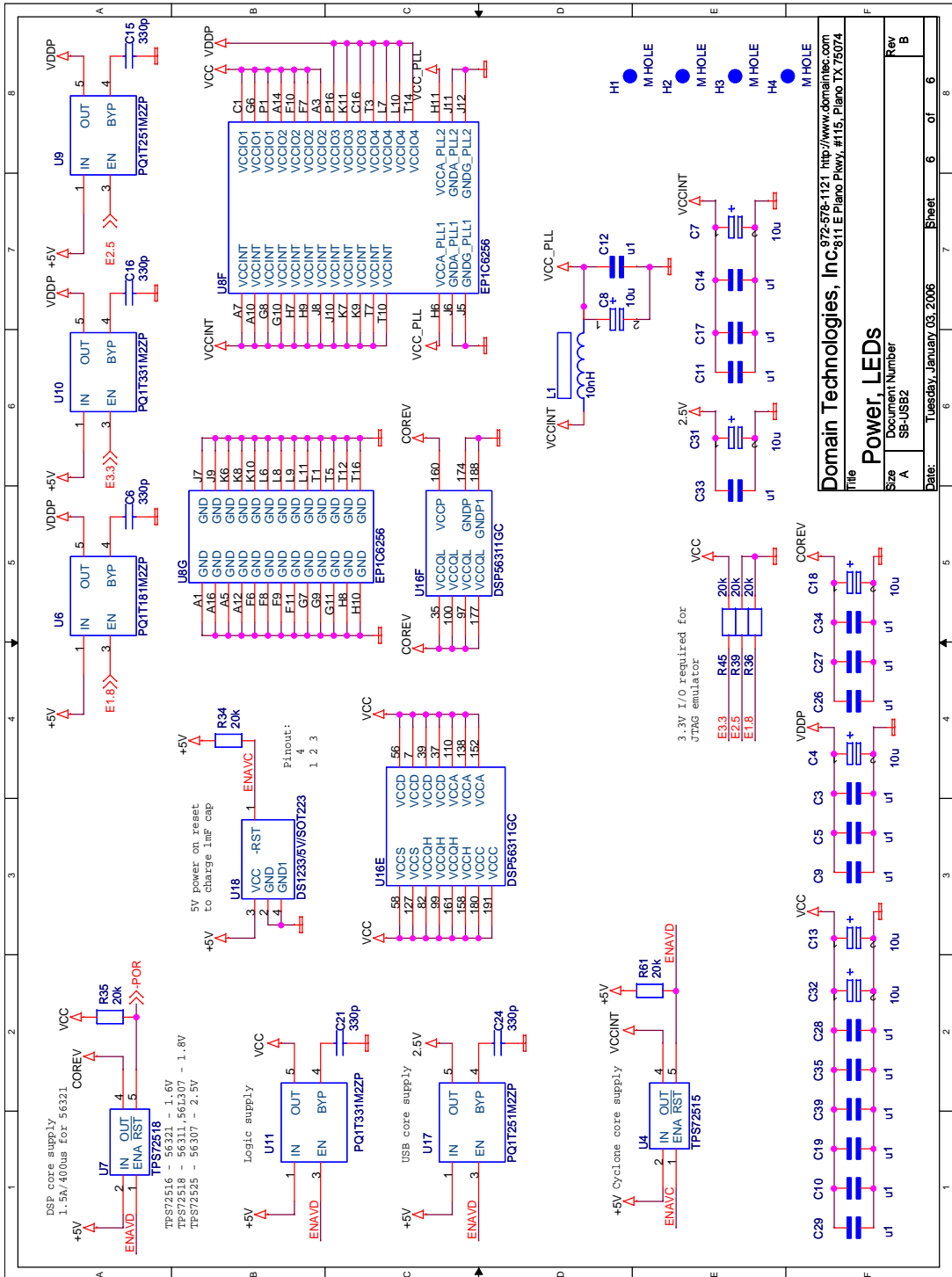


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Required for 96321

External power connector for more than 500 mA configurations
 Pinout:
 1 2 3
 4

Panasonic
 EEV-HA0J102UP
 600 mA current
 1.1 limiter



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File: Power_LEDS

Size: Document Number: SB-USBZ

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