SB-56K

Multi DSP Emulator

Product of Domain Technologies, Inc.

SB-56K User's Guide,

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CHAPTER 1

Introduction

The development system for Motorola's DSPs consists of the following components:

- SB-56K main emulator unit
- BoxView - Debugger Graphical User Interface
- BoxServer (optional) server used for remote, multiple device and/or multiple user access

First component will be described in the following chapters.
BoxView debugger and BoxServer documentation can be found in the separate manuals.
Software components need to be installed first.
System software requires 32-bit operating system (Windows 95/98/NT/2000).
System software can not be run on earlier versions of the Windows PC operating system (Win 3.1, 3.11), even if the Win 3.2s option is installed.

1.1 - SB-56K Front View

FIGURE 1.1.

1.2 - SB-56K Back View

FIGURE 1.2.

1.3 - SB-56K circuitry

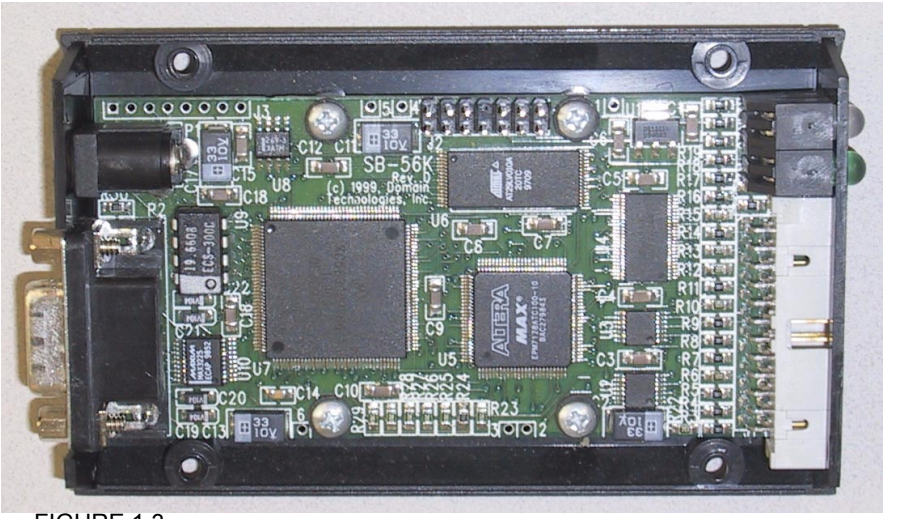

FIGURE 1.3.

CHAPTER 2

Hardware Description

2.1 - Package Contents

Complete emulator unit consists of the following components:

- SB-56K emulator box
- 5 VDC power supply
- DB9F/DB9M RS-232 Cable
- DB25F/DB9M conversion module
- IDC24/IDC14 JTAG/OnCE ribbon emulation cable
- IDC24/IDC14/IDC14 Dual OnCE “Y” ribbon emulation cable

2.2 - JTAG Emulation cable

Emulator is connected to the target system with the 24/14 ribbon cable. Pinout of the 14-pin header is as follows:

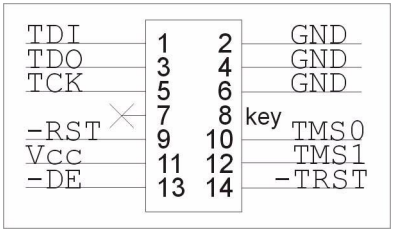

FIGURE 2.1.

The required connections are: TDI, TDO, TCK and TMS0. TDI is data output to the target device(s). TDO is JTAG data input from the target devices to the emulator.

TMS0 is the default Test Mode Select control signal. The TMS1 signal allows to control secondary scan-chain, which could be connected in parallel to the primary one.

The -DE signal is optional. Is not used for the basic emulation control, but can be used as a signal to control emualator's benchmark timer.

To prvent against accidental reverse connection, pin number 8 of the JTAG header on the trget board should be removed. Connecting the emulation cable to the target board in the reverse direction (pin #1 as a pin #14), can damage emulator's circuitry.

For the proper reset sequence, -TRST and -RESET signals should not be connected together on the target board. Options for connecting those two signals together are described in the chapter 2.5.

Description of the emulation header signals:

Pin #	Signal Name	Description
1	TDI	JTAG Data In
3	TDO	JTAG Data Out
5	TCK	JTAG Clock
9	-RESET	DSP HW Reset
10	TMSO	JTAG Test Mode Select
11	VCC	Target VCC
12	TMS1	Secondary TMS
13	-DE	DSP Debug Event
14	-TRST	JTAG Reset
2,4,6	GND	Signal ground
7	NC	Not Connected
8	Key	Pin #8 removed

2.3 - Dual OnCE Emulation cable

Dual OnCE version of the SB-56K emulator is equipped with 24 pin connector. Supplied “Y” cable allows to connect two independent OnCE devices.

Some signals are shared between JTAG and OnCE operation modes. For proper dual OnCE operation, pins 10, 12 and 14 of the primary OnCE header should not be connected to ground.

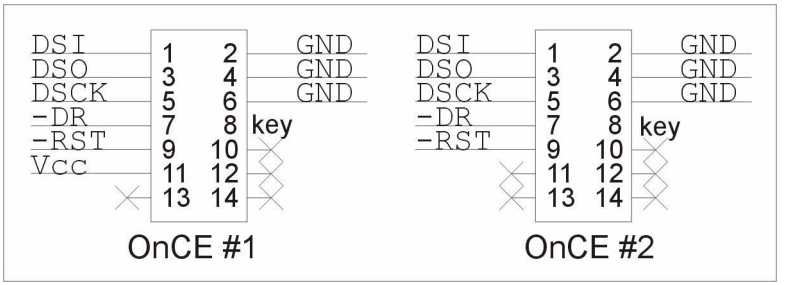

FIGURE 2.2.

Cable has two 14 pin connectors.
Connector #1 has 14 wire ribbon cable.
Connector #2 is installed on 10 wire section of the ribbon cable.

Target’s Vcc can be detected by the emulator through pin #11 of the OnCE header #1.

Target’s Vcc is not required for the proper emulator’s operation.

2.4 - Emulator LEDs

TABLE 1.

1	TOP LEFT	GREEN	EMULATOR POWER
2	BOTTOM LEFT	RED	JTAG MODE
3	TOP RIGHT	RED/GREEN	STATUS 2
4	BOTTOM RIGHT	RED/GREEN	STATUS 1

On the front panel of the SB-56K are installed 4 status LEDs:

Led #2 reflects current emulator status:

TABLE 2.

LED ON	JTAG MODE
LED OFF	OnCE MODE
LED BLINKING	Emulator not initialized

In the OnCE mode, lower right LED reflects status of the device #1, the top right LED shows status of the second device.

LED turned off indicates that the device is not initialized or executing user code. If the target device was stoped through the HALT command or hit a software breakpoint, LED will be set to red. In case of the hardware breakpoint or single step mode, LED will be set to green.

In the JTAG mode, lower right LED indicates last status change of the target device.

LED turned off indicates that the emulator issued RUN command.

If the last event was getting into debug mode because of the hardware breakpoint or OnCE trace counter, LED will be set to green.

If one of the target devices entered debug mode through emulator HALT command or software breakpoint, LED will be set to red.

2.5 - Target reset requirements

Target system reset should be performed by asserting both -DSPRESET and -TRST signals at the same time.

Emulator needs to control both of the reset signals independently. During active -DSPRESET emulator needs to access JTAG port to set proper state of the TAP controller.

To satisfy above requirements Target system needs to incorporate following logic (this can be a part of the PLD, or discrete logic):

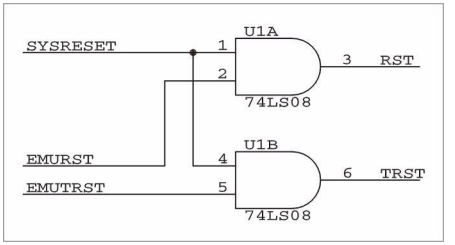

FIGURE 2.3.

Above effect can be accomplished also with a very simple circuit:

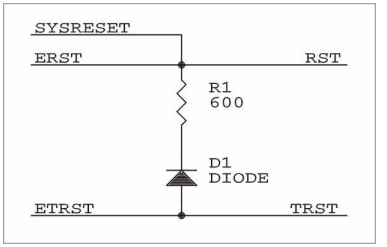

FIGURE 2.4.

2.6 - Emulation clock

JTAG or OnCE emulation clock can be controlled in range of 8 MHz to 8 kHz. The default TCK value is 2 MHz. Slower clock can be needed for target devices operating at lower clock frequencies, or for systems with “noisy” TCK lines. Noise of the TCK can cause the JTAG state machine to get corrupted.

The frequency of the emulation clock can be set or checked with the BoxView’s TCLOCK command. Changes of the TCK frequency are stored within the emulator hardware, and will be restored on the next system initialization.

The actual clock value can be set only to specific frequencies. BoxView software finds the closest value possible, and displays its exact value.

2.7 - Benchmark timer

Emulator allows to measure target execution time. This option is available only in the JTAG mode of operation.
Emulator’s counter is started when the target device is set into the RUN mode. Counter is stopped with the -DE signal from the target. Counter is driven by the internal emulator clock, which is 4x frequency of the TCK signal.

For multiple target devices benchmark feature can be enabled or disabled with the BENCHMARK command.
The last execution time is displayed on the debugger’s status line (bottom of the application window). The status line shows only most significant digits in time format: hh:mm:ss.msec.usec. Full time value and exact value of the benchmark counter is available with the BENCHMARK command.

2.8 - RS-232 baud rate.

Emulator initializes at 9600 baud. The baudrate can be changed with the BAUD command or from the Baud Rate selection dialog available in the Options pull down menu. The last set baudrate is saved in the .ini file, and on the next system initialization it will be restored.

Emulator supports baud rates up to 460 kbaud. The baud rate selection depends on the capabilities of the host PC.

CHAPTER 3 ***Schematics***

SB-56K Circuit Diagram (1 of 3) ***Figure on page 13***

SB-56K Circuit Diagram (2 of 3) ***Figure 2 on page 15***

SB-56K Circuit Diagram (3 of 3) ***Figure 3 on page 16***

Quad Jtag adaptor ***Figure 4 on page 17***

Probe-56001 ***Figure 5 on page 18***

TABLE 1. SB-56K Circuit Diagram (1 of 3)

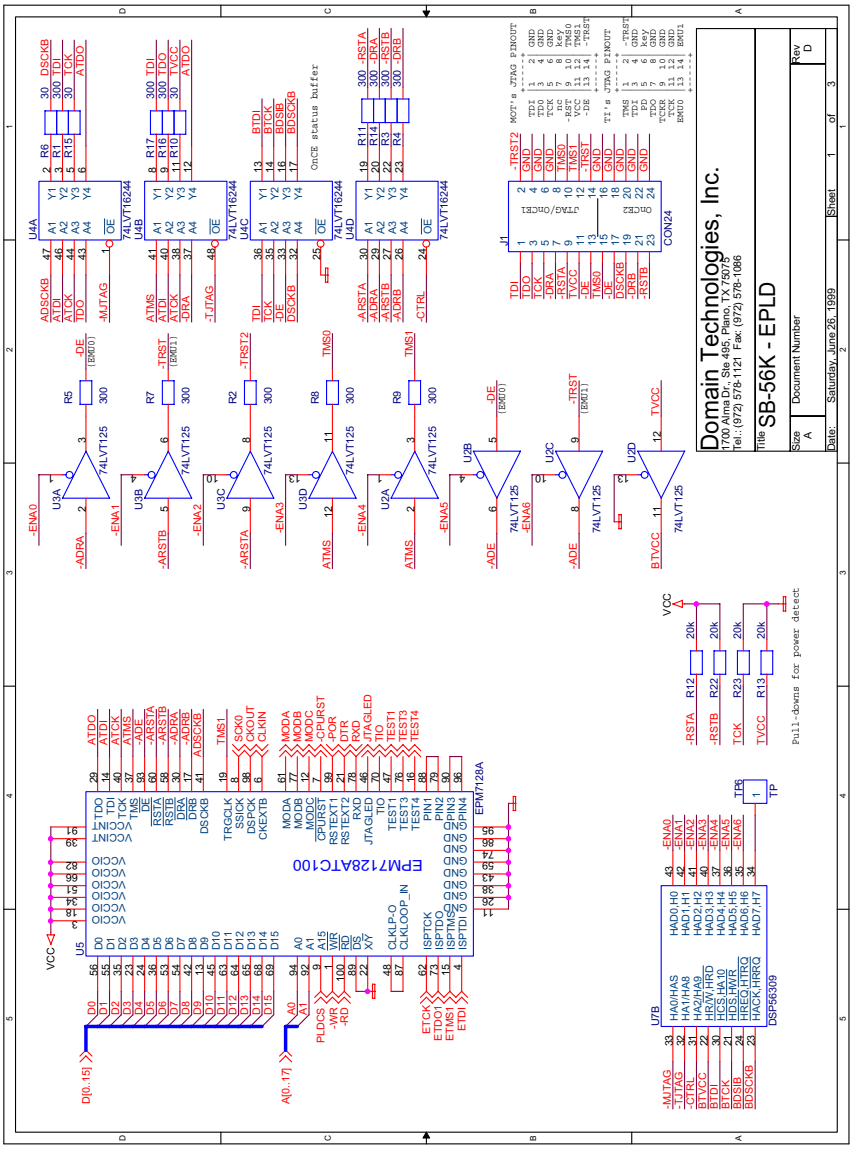

TABLE 2. SB-56K Circuit Diagram (2 of 3)

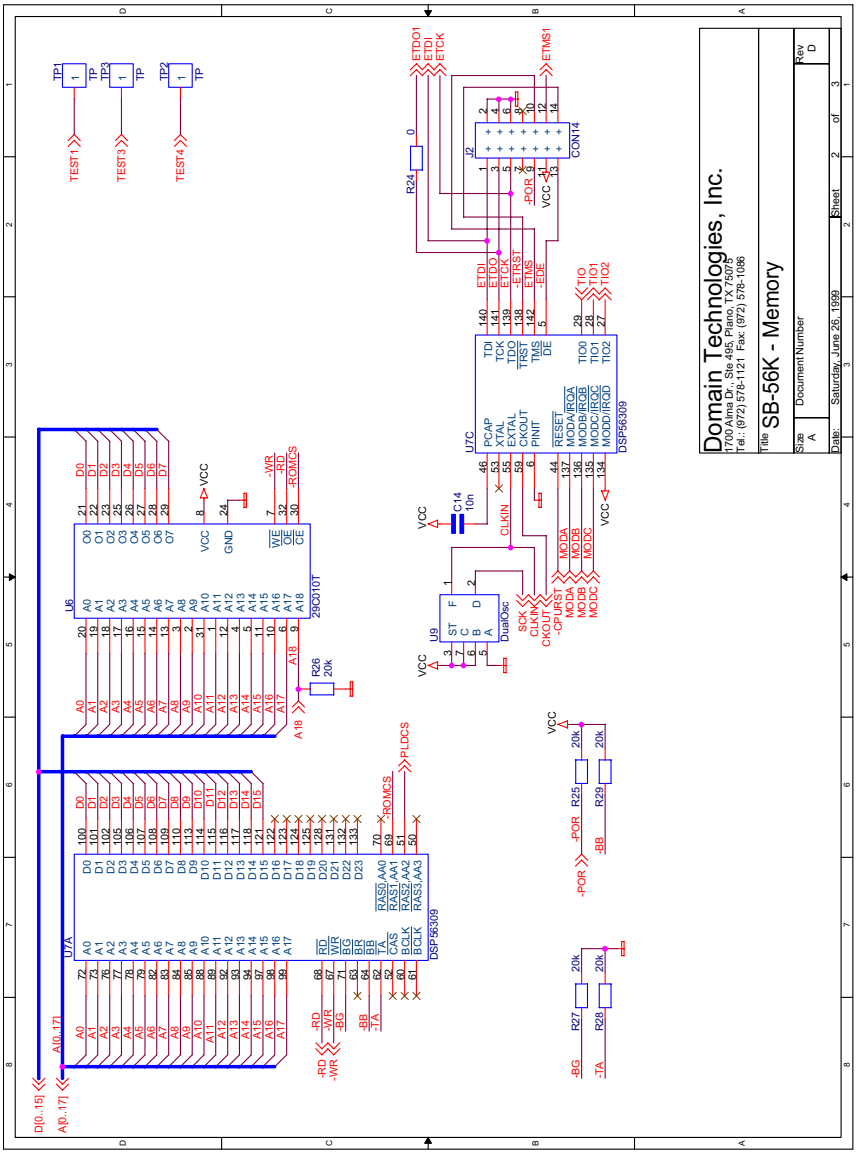

TABLE 3. SB-56K Circuit Diagram (3 of 3)

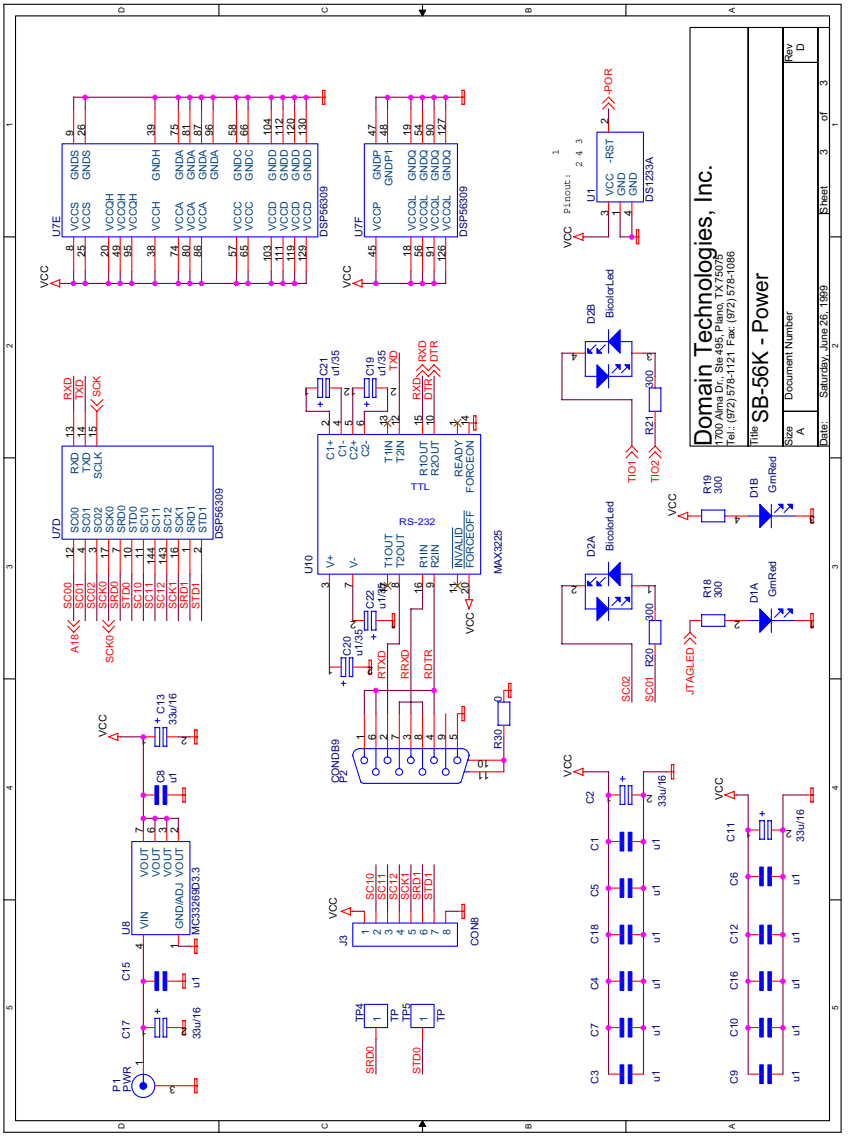

TABLE 4. Quad Jtag adaptor

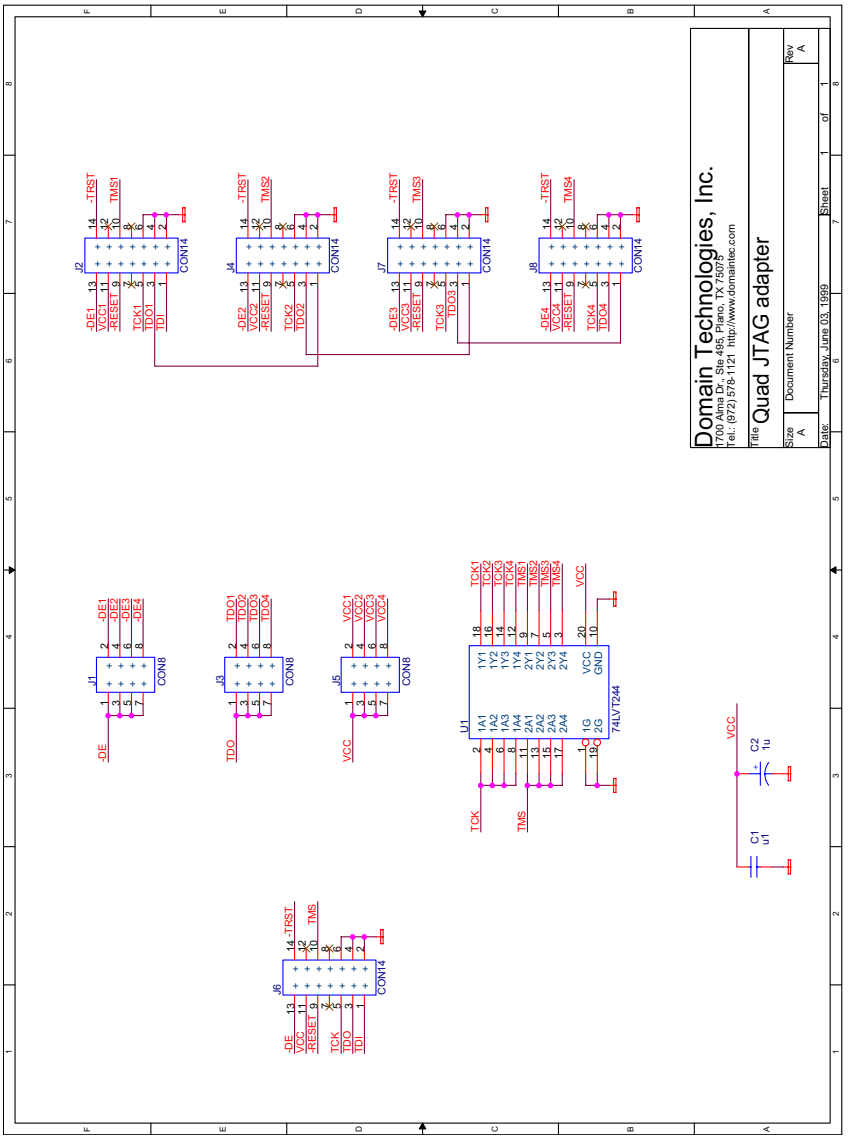

TABLE 5. Probe-56001